IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD. ET AL., Defendants.	Case No. 2:22-cv-293-JRG (Lead Case) JURY TRIAL DEMANDED
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-cv-294-JRG JURY TRIAL DEMANDED

DEFENDANT MICRON'S RESPONSE TO PLAINTIFF NETLIST'S MOTION FOR SUMMARY JUDGMENT THAT THE ASSERTED PATENTS ARE NOT STANDARD ESSENTIAL

[redacted]

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I. INTRODUCTION

Defendants ("Micron") oppose Plaintiff's ("Netlist") motion for summary judgment that the Asserted Patents are not standard essential ("Motion"). Netlist's entire infringement theory is predicated on U.S. Patent No. 7,619,912 (the "'912 patent") and U.S. Patent No. 11,093,417 (the "'417 patent") (collectively, the "Asserted Patents") being standard essential, given Netlist relies on logic diagrams from JEDEC specifications, which are ***admittedly optional***, to prove infringement of certain claimed circuitry elements in both Asserted Patents, with no analysis of the Accused Products' internal circuitry. Netlist further fails to prove that implementing these logic diagrams from the JEDEC specification would always result in infringement, given these logic diagrams do not represent actual circuits or how the Accused Products' internal circuit components are implemented. Netlist has not proffered any evidence that these logic diagrams are the only possible structure for a standard compliant product, that the actual circuitry in the Accused Products uses that design, or that designing an actual circuit based on these logic diagrams would necessarily result in infringement.

Additionally, although Netlist's infringement expert includes some references to third-party datasheets in his analysis, these datasheets simply recycle the same high-level, optional logic diagrams. And he fails to address all third-party suppliers whose components are used in the Accused Products to purportedly infringe, relying strictly on their standard compliance in his analysis.

Netlist cannot have it both ways. Either the patents are standard essential and standard compliance may be a way to prove infringement; or the patents are not standard essential and Netlist has failed to meet its burden of proof on infringement as a matter of law. Because Netlist's infringement theory is predicated on a finding that the Asserted Patents are standard essential, the Court should deny Netlist's Motion or, in the alternative, grant Micron's co-pending Motion for

Summary Judgment of Non-Infringement finding that Netlist failed to meet its burden of proof on infringement as a matter of law.

II. RESPONSE TO STATEMENT OF ISSUE TO BE DECIDED

There are two issues before the Court. The first is whether the Court should deny Netlist's Motion for Summary Judgment that the '912 patent and '417 patent are not standard essential because there are genuinely disputed material facts that suggest otherwise. The second is, if the Court chooses to grant Netlist's Motion, whether doing so also requires granting Micron's co-pending Motion for Summary Judgment of Non-Infringement because Netlist has not shown that the circuitry in the Accused Products infringes and because Netlist has proffered no evidence other than the standard-referenced design to meet its burden of proof on infringement as a matter of law.

III. RESPONSE TO NETLIST'S STATEMENT OF UNDISPUTED MATERIAL FACTS

Micron responds to Netlist's statement of undisputed material facts as follows.

1) Admitted. Micron, however, disputes Netlist's assertions to the extent that it intends to suggest that these definitions and statements are dispositive of whether the Asserted Patents are essential to the standard.

2) Micron disagrees with Netlist's assertion that "Netlist does not contend that the '417 Patent is standard essential or that claim 16 of the '912 Patent, the lone asserted claim, is standard essential." Micron also disagrees with Netlist's assertions that "Netlist's experts expressly opine the Asserted Patents are not standard essential." To the contrary, Netlist and its experts expressly rely on optional diagrams from the JEDEC standards to prove infringement, thus requiring that these claims are standard essential under its theory, as described further in subsequent sections.

[redacted]

3) Micron admits that figures or diagrams in JEDEC specifications are not required portions of the standard, [redacted]. Relevant to this Motion, Micron admits that the JEDEC logic diagrams relied upon by Dr. Mangione-Smith in his infringement analysis are not required portions of the standard.

IV. ARGUMENT

Courts should grant summary judgment only if the evidence "shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a); *see also Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986). Thus, to rebut such a motion, "all that is required is that sufficient evidence supporting the claimed factual dispute be shown to require a jury or judge to resolve the parties' differing versions of the truth at trial." *Scripps Clinic & Rsch. Found. v. Genentech, Inc.*, 927 F.2d 1565, 1571 (Fed. Cir. 1991) (citation omitted). "[T]he inferences to be drawn from the underlying facts contained in such materials must be viewed in the light most favorable to the party opposing the motion." *United States v. Diebold, Inc.*, 369 U.S. 654, 655 (1962).

A. Netlist's Infringement Positions Require a Finding That the Patents Are Standard Essential or, in the Alternative, That Netlist Has Failed to Meet Its Burden of Proof on Infringement as a Matter of Law

Netlist has repeatedly taken conflicting positions on whether the Asserted Patents are standard essential in this case. On the one hand, Netlist brings this Motion to establish that the patents are not standard essential as a matter of law. On the other hand, Netlist relies on optional sections of the JEDEC standard to prove infringement of certain claimed circuitry elements in both Asserted Patents, without comparing the patent claims to the different Accused Products and without showing that practicing the standard would necessarily result in infringement. Netlist cannot have it both ways. Either the patents are standard essential and standard compliance may

[redacted]

be a way to prove infringement or the patents are not standard essential and Netlist has failed to meet its burden of proof on infringement as a matter of law.

The Federal Circuit in *Fujitsu* held that compliance with an industry standard may be sufficient to establish patent infringement. *Fujitsu Ltd. v. Netgear Inc.*, 620 F.3d 1321, 1327 (Fed. Cir. 2010). However, the Federal Circuit raised two important caveats. First, the Federal Circuit explained that when a relevant section of the standard is optional, the patent owner must (1) compare the claims to the accused products or (2) if appropriate, prove that the accused products implement any relevant optional sections of the standard:

> [***When***] ***the relevant section of the standard is optional***, [] standards compliance alone would not establish that the accused infringer chooses to implement the optional section. In these instances, it is not sufficient for the patent owner to establish infringement by arguing that the product admittedly practices the standard, therefore it infringes. ***In these cases, the patent owner must*** [*1*] ***compare the claims to the accused products or,*** [*2*] ***if appropriate, prove that the accused products implement any relevant optional sections of the standard.*** This should alleviate any concern about the use of standard compliance in assessing patent infringement. Only in the situation where a patent covers every possible implementation of a standard will it be enough to prove infringement by showing standard compliance.

Id. at 1327-28. (emphases added).

Second, the Federal Circuit explained that it is only "appropriate" to use an industry standard to prove infringement when the standard provides the level of specificity required to show that practicing the standard would always result in infringement.

> [***I***]***n many instances, an industry standard does not provide the level of specificity required to establish that practicing that standard would always result in infringement*** . . . . In these instances, it is not sufficient for the patent owner to establish infringement by arguing that the product admittedly practices the standard, therefore it infringes . . . . ***Only in the situation where a patent covers every possible implementation of a standard will it be enough to prove infringement by showing standard compliance.***

[redacted]

Id. (emphases added).

1. Netlist relies on admittedly optional logic diagrams from the JEDEC standards to prove infringement of certain claimed circuitry elements.

Netlist's infringement theory relies on ***admittedly optional*** logic diagrams from the JEDEC standards to prove infringement of certain claimed circuitry elements, without any corresponding analysis of the Accused Products. And in fact, Netlist even admits that these features and logic diagrams are optional in its Motion.

For example, claim 16 of the '912 patent (the only asserted '912 patent claim) and claim 1 of the '417 patent (the only independent '417 patent claim) claim a memory module that has specific circuitry—including, for example:

> [16.f] the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, and
>
> [16.i] a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

Claim 16, '912 patent.

> [1.d] circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module.

Claim 1, '417 patent.

Dr. Mangione-Smith, Netlist's infringement expert, contends that [redacted]

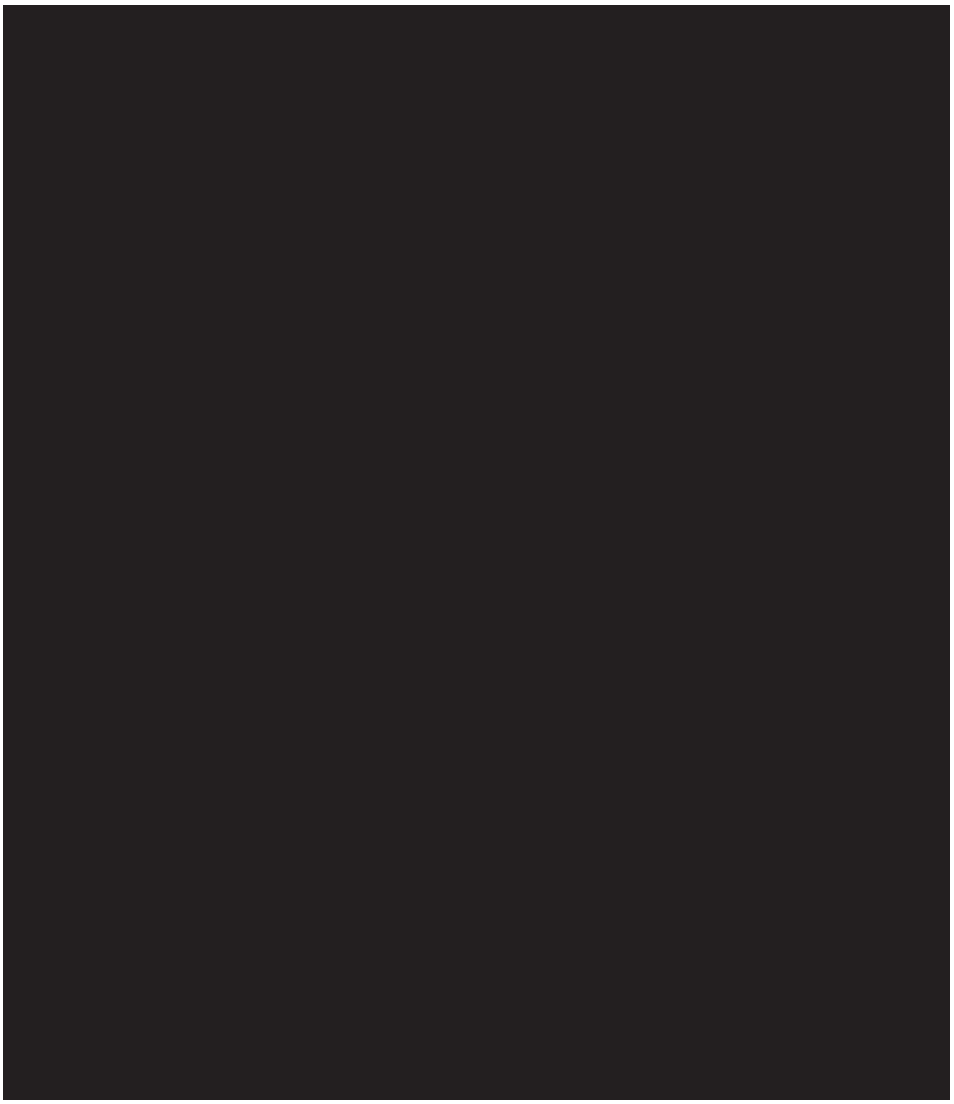
[redacted]

Ex. 1 (Mangione-Smith Rpt.) at Ex. B (¶¶ 42-46, 56-59), Ex. C (¶¶ 95-135). [redacted] RCDs and data

[redacted]

buffers used in the Accused Products generally adhere to JEDEC specifications [redacted] respectively. *Id.* at Ex. A (¶¶ 69-70); [redacted].

In support of his opinion that the RCDs and data buffers in the Accused Products include this specific circuitry required by limitations [16.f] and [16.i] of the '912 patent and limitation [1.d] of the '417 patent, and thus infringe these claim elements, Dr. Mangione-Smith relies entirely on two logic diagrams from JEDEC specifications [redacted] as shown below:



[redacted] at 66 (the "[redacted] RCD Logic Diagram"); Ex. 1 (Mangione-Smith Rpt.) at Ex. B (¶¶ 43-44) (relying on figure in JEDEC specification for infringement for limitation 16[f] of '912 patent), (¶ 58) (relying on figure in JEDEC specification for infringement for limitation 16[i] of '912 patent).

[redacted]

[redacted] at 95 (the "[redacted] Data Buffer Logic Diagram"); Ex. 1 (Mangione-Smith Rpt.) at Ex. C (¶¶ 99, 102, 110, 123) (relying on figure for infringement of limitation 1[d] of the '417 patent).

Netlist, ignoring its own reliance on these exact logic diagrams in its expert reports and infringement theory, argues that the Asserted Patents are not standard essential because these logic diagrams are optional to the standard:

> [T]he portions of the JEDEC standard Dr. Stone points to are not required. As discussed above, the logic diagram [redacted] is not required, and the same is true for the logic diagram [redacted].

[redacted]

Mot. at 8, 2 (Undisputed Fact No. 3).

Netlist finds support for its position that the [redacted] RCD Logic Diagram and the [redacted] Data Buffer Logic Diagram are optional from various sources. For example, Netlist finds support that these logic diagrams are optional from Micron's corporate representatives:

> Micron's corporate representative admitted that logic diagrams in the JEDEC specifications such as the one Dr. Stone refers to are ***not*** required portions of the standard. [redacted]

Mot. at 7.

> Micron's own corporate representative, [redacted], admitted [that the logic diagram [redacted] is not required, and the same is true for the logic diagram of [redacted]]. [redacted]

Mot. at 8-9.

Netlist also finds support that the [redacted] RCD Logic Diagram and the [redacted] Data Buffer Logic Diagram are optional from its own experts:

> Netlist's experts also explain that the portions of the JEDEC specification Dr. Stone points to are not required. For example,

[redacted]

> Dr. Mangione-Smith explains that the JEDEC standard [redacted] Ex. 2 (Mangione-Smith Rebuttal, Ex. B) at ¶ 577-578. He further explains [redacted] *Id.* at ¶ 579. ***Mr. Gillingham likewise opines that both of the logic diagrams pointed to by Dr. Stone are only exemplary and are not required by the standard.*** Ex. 3 (Gillingham Rebuttal Rpt.) at ¶¶ 121 [redacted]. Micron does not refute this.

Mot. at 9 (emphases added).

> Netlist's experts confirm [that logic diagrams in the JEDEC specifications such as the one Dr. Stone refers to are not required portions of the standard]. For example, Netlist's JEDEC expert Mr. Gillingham explains that [redacted] Ex. 3 (Gillingham Rpt.) at ¶ 119. Mr. Gillingham further explains that the exact logic diagram Dr. Stone points to [redacted] *Id.* at ¶ 125. Micron does not rebut this analysis.

Mot. at 7.

Given both parties agree—and Netlist affirmatively argues in its Motion—that the [redacted] RCD Logic Diagram and the [redacted] Data Buffer Logic Diagram are optional sections of JEDEC specifications [redacted], respectively, it is undisputable that these logic diagrams are ***optional***.

Further, Dr. Mangione-Smith points to ***no other evidence*** beyond these two optional logic diagrams to purportedly show the internal circuitry of the Accused Products' RCDs and data buffers, or how any of the internal circuit components are implemented. Although Dr. Mangione-Smith includes some references to third-party RCD and data buffer data sheets in his analysis, these references simply recycle the ***same logic diagrams copied and pasted from the standard***.

[redacted]

Therefore, Netlist undisputedly relies on optional logic diagrams from the JEDEC standards to prove infringement of the Asserted Patent claims.

2. The optional logic diagrams that Netlist relies on from the JEDEC standards lack the level of specificity required to establish that practicing the standard would always result in infringement.

In addition to being undisputedly optional sections of the JEDEC standard, the two logic diagrams that Netlist relies upon to prove infringement of certain claimed circuitry elements—the [redacted] RCD Logic Diagram and the [redacted] Data Buffer Logic Diagram—lack the level of specificity required to establish that practicing the standard would always result in infringement. *See Fujitsu*, 620 F.3d at 1327-28. This is because these logic diagrams do not reflect the actual circuitry in the Accused Products' RCDs or data buffers and do not show how the components are actually implemented, as the testimony explains below. Thus, Dr. Mangione-Smith erred in making a conclusory statement without evidence that all buffers and RCDs in the Accused Products have [redacted] as these logic diagrams. Ex. 1 (Mangione-Smith Rpt.) at Ex. A (¶ 57).

Two witnesses—one from Micron and another from a third-party supplier, [redacted] explain that these JEDEC logic diagrams and the logic diagrams in the data sheets do not reflect the actual circuitry in RCDs or data buffers. [redacted] corporate representative explained that the

[redacted]

[redacted]

[redacted] at 20:24-21:15 (emphases added).

Similarly, Micron's corporate representative, [redacted], explained that the same logic diagrams do not specify how the different circuitry components can be implemented.

[redacted] at 109:1-19 (emphases added).

Dr. Stone also confirms that the logic diagrams from the JEDEC standards do not show the internal circuitry of RCDs and data buffers used in Micron's accused products. Ex. 6 (Stone Rpt.) ¶¶ 58 [redacted], 54-63.

Netlist has not proffered any evidence that these logic diagrams are the only possible structure for a standard compliant product, or that designing an actual circuit based on these logic diagrams would always result in infringement. Because these logic diagrams do not reflect actual circuitry and do not reflect how circuitry components are actually implemented, these logic diagrams "do[] not provide the level of specificity required to establish that practicing that standard would always result in infringement." *Fujitsu*, 620 F.3d at 1327.

[redacted]

3. Netlist has failed to compare the claims of the Asserted Patents to the Accused Products.

Because the [redacted] RCD Logic Diagram and the [redacted] Data Buffer Logic Diagram—the two logic diagrams that Netlist relies upon to prove infringement of certain claimed circuitry elements including limitations [16.f] and [16.i] of the '912 patent and limitation [1.d] of the '417 patent—are undisputedly optional, Netlist was required to "[1] compare the claims to the accused products or, [2] if appropriate, prove that the accused products implement any relevant optional sections of the standard." *See Fujitsu*, 620 F.3d at 1327-28. Netlist failed to do either.

First, Netlist failed to compare the Asserted Patent claims to the Accused Products. Dr. Mangione-Smith simply relies on these two optional logic diagrams and accompanying high-level tables from the JEDEC standard to assert that the Accused Products have internal circuitry that includes the claimed circuitry elements. But as previously stated, numerous witnesses have explained that these logic diagrams do not reflect the actual circuit design of an RCD or data buffer and do not specify how the different circuitry components are implemented. *See* Sections IV.A.1, IV.A.2, *supra*. Therefore, relying on these high-level, optional logic diagrams does not prove that any circuit from the Accused Products includes the claimed circuitry elements.

Further, although Dr. Mangione-Smith includes some references to third-party RCD or data buffer data sheets in his analysis, he simply recycles the same exact high-level logic diagram from the standard when showing the RCDs' and data buffers' internal circuitry—namely, the [redacted] RCD Logic Diagram and the [redacted] Data Buffer Logic Diagram. *See* Ex. 1 (Mangione-Smith Rpt.) at Ex. B (¶ 44), Ex. C (¶¶ 26, 31, 56). Therefore, these third-party references suffer from the same fundamental flaw. Dr. Mangione-Smith provides no evidence of how the internal circuits are designed or internal circuitry components are implemented for these RCDs or data buffers.

[redacted]

Additionally, Dr. Mangione Smith admits that Micron sources its DDR4 RCDs and data buffers from [redacted] Ex. 1 (Mangione-Smith Rpt.) at Ex. A (¶¶ 58-60). This is undisputed. However, Dr. Mangione-Smith only analyzes [redacted] RCDs and data buffers for the claimed circuitry elements of the '912 patent. *Id.* at Ex. B (¶ 44). Dr. Mangione-Smith did not analyze [redacted] or [redacted] RCDs and data buffers for the claimed circuitry elements of the '912 patent. And Dr. Mangione-Smith only analyzes [redacted] and [redacted] and data buffers for the claimed circuitry elements of the '417 patent. *Id.* at Ex. C (¶¶ 96, 102, 104-105, 107, 109, 112-114, 117, 121, 122, 130-132, 184). Dr. Mangione-Smith did not analyze [redacted] RCDs and data buffers for the claimed circuitry elements of the '417 patent. Dr. Mangione-Smith justifies this decision with a conclusory statement that he understands all DDR4 RCDs and DDR4 data buffers used in Micron's Accused Products to [redacted] *Id.* at Ex. A (¶¶ 59-60). But his purported understanding relates only to the fact that these components are standard compliant. The logic diagrams do not reflect the actual circuit design of an RCD or data buffer and do not specify how the different circuitry components are implemented. Therefore, citing these high-level logic diagrams in one supplier's third-party data sheet to claim to show the internal circuitry of that RCD or data buffer does not mean that other third-party RCDs and data buffers implement the same internal circuitry. Netlist simply relies on the fact that these other third-party components are standard compliant to assert that the circuitry is the same, which directly contradicts its claim that the Asserted Patent claims are not standard essential.

Second, Netlist failed to prove that complying with these logic diagrams from the JEDEC standards always results in infringement, given these logic diagrams do not represent actual

circuits or how components are implemented. Netlist has not proffered any evidence that these logic diagrams represent the only possible structure for a standard compliant product, or that designing an actual circuit based on these logic diagrams would always result in infringement. Therefore, these logic diagrams lack the level of specificity required by *Fujitsu*. *See* 620 F.3d at 1327-28. Setting aside Dr. Mangione-Smith's failure to address [redacted] and [redacted] for the '912 patent's claimed circuitry elements and failure to address [redacted] for the '417 patent's claimed circuitry elements, Netlist's reliance on third-party data sheets that simply cut and paste these high-level JEDEC logic diagrams into the data sheets similarly lacks the level of specificity required by *Fujitsu*, and it is insufficient to show the actual circuitry of the third-party RCDs and data buffers.

Because Netlist failed to compare the claims of the Asserted Patents to the Accused Products, failed to show that practicing the standard as it relates to these logic diagrams always results in infringement, and failed to analyze all types of RCDs and data buffers used in the Accused Products, Netlist's infringement analysis requires a finding that the Asserted Patent claims are standard essential or, in the alternative, that Netlist has failed to meet its burden of proof on infringement as a matter of law.

B. Netlist Mischaracterizes Micron's Arguments as an "If Infringed, Then Essential" Opinion

Given the fundamental flaws in Dr. Mangione-Smith's infringement analysis as it relates to reliance on JEDEC standards, Netlist desperately attempts to discredit Micron's position with mischaracterizations. For example, Netlist takes Micron's statements out of context to mischaracterize Micron's position as an "If Infringed, Then Essential" opinion. *See* Mot. at 3. But this is simply not true. As Dr. Stone states in his Report, Micron's position is that [redacted]

[redacted] Ex. 6 (Stone Rpt.) at ¶ 398 (emphasis added). In other words, to the extent Netlist is allowed to prove infringement by relying on the JEDEC standards without corresponding analysis of the Accused Products, despite Netlist repeatedly admitting that these sections and diagrams from the JEDEC standard are optional and despite Netlist offering no evidence that circuitry complying with these optional diagrams would always result in infringement, the claims must be found essential to the JEDEC standards. Netlist's reliance on optional sections of the JEDEC standard to prove infringement requires a finding either that the patents are standard essential or that there is no proof of infringement.

Further, Netlist disingenuously argues that Micron "has no evidence or technical analysis sufficient to meet its burden on essentiality." Mot. at 5 (emphasis removed). However, this is simply not true. Netlist has already performed that analysis in its infringement contentions when it mapped every single asserted claim of both the '912 patent and the '417 patent to the JEDEC standards. Ex. 7 (Netlist Infringement Contentions) at Ex. A-1, Ex. B. Dr. Stone's Report makes clear that he reviewed and incorporated by reference Netlist's infringement contentions mapping all claims to the JEDEC standards.

[redacted]

Ex. 6 (Stone Rpt.) at ¶ 404 (emphasis added). Dr. Stone's Report explains that, assuming Dr. Mangione-Smith's infringement theory is correct, every single limitation for claims 1 and 16 of the '417 and '912 patents is required by a few JEDEC standards, collectively, thus making the claims standard essential. *Id.* at ¶¶ 399-403. Netlist's argument that Dr. Stone's Report contains "no analysis comparing each element of claim 16 of the '912 Patent to the JEDEC standards" and

[redacted]

"no analysis comparing each element of the claims of the '417 Patent to the JEDEC standards," merely because Dr. Stone did not duplicate Netlist's infringement contentions, is disingenuous. *See* Mot. at 5, 8. Netlist's infringement contentions are plainly written to the JEDEC standards and support a factual finding that the claims are standard essential under Netlist's broad infringement read.

Similarly, Dr. Mangione-Smith also mapped the asserted claims to the relevant JEDEC standards—albeit not as explicitly as in Netlist's original infringement contentions. That is, in Dr. Mangione-Smith's Expert Report, he switches out the express JEDEC standards used in Netlist's infringement contentions for data sheets and schematics for Micron and third-party products that Dr. Mangione-Smith concedes are compliant with JEDEC standards, including some of the original JEDEC standards relied upon to show infringement in Netlist's infringement contentions. *See* Ex. 1 (Mangione-Smith Rpt.) at Ex. A (¶ 69) ([redacted] Netlist's infringement allegations for the '912 patent and '417 patent clearly hinge on the Relevant JEDEC Standards, whether expressly, as shown in Netlist's infringement contentions, or implicitly, as shown in Dr. Mangione-Smith's Expert Report. In both Netlist's infringement contentions and Dr. Mangione-Smith's Report, Netlist relies upon either actual JEDEC standards or data sheets for JEDEC-compliant Micron and third-party products to map every single element of the claims for infringement. *See* Ex. 7 (Netlist Infringement Contentions) at Ex. A-1, Ex. B.

[redacted]

At bottom, it is Netlist's reliance solely on optional sections of the JEDEC standard to prove infringement that necessarily requires a finding that the Asserted Patents are standard essential, or that Netlist has failed to prove infringement. *Fujitsu*, 620 F.3d at 1327-28.

C. Netlist's Reliance on Judge Payne's Decision in the -203 Litigation Is Misplaced

Netlist also argues that the Court should grant its Motion because "[t]his Court recently rejected the exact same argument in the co-pending litigation with Micron" that Micron presents here, which is simply not true. Mot. at 3. Unlike the co-pending litigation (Case No. 22-cv-203) ("the -203 Litigation"), here, Netlist has admitted and affirmatively argued that the JEDEC logic diagrams it relies on to show infringement are ***completely optional*** but did not undertake to analyze the actual Accused Products, unlike in the co-pending litigation. Mot. at 7-9. This presents a unique situation requiring a finding that the patents are standard essential or, in the alternative, that Netlist's infringement theory must fail as a matter of law for the reasons explained in Section IV.A. In the -203 Litigation, neither party made such an argument or admission. Dkts. 276, 305, 344, 370. Further, Netlist's own counsel even admits that the case here is different than the -203 Litigation:

[redacted]

[redacted]

Ex. 8 (Claim Construction Tr.) at 8:6-9:11.

[redacted]

Id. at 108:16-22.

Thus, Netlist's reliance on Judge Payne's decision in the -203 Litigation is misplaced.

V. CONCLUSION

For the reasons stated above, the Court should deny Netlist's Motion for Summary Judgment that the Asserted Patents are not standard essential. If the Court decides to grant Netlist's Motion, however, it must also grant Micron's Motion for Summary Judgment of non-infringement of the '912 and '417 patents because Netlist failed to satisfy its burden of proof on infringement as a matter of law.

Dated: January 30, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on January 30, 2024, the foregoing document was electronically filed with the Clerk of Court using the Court's CM/ECF system, which will send notification of such filing to all counsel of record, including counsel of record for Plaintiff Netlist Inc.

/s/ Michael R. Rueckheim
Michael R. Rueckheim

CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL

I hereby certify that the foregoing document and exhibits attached hereto are authorized to be filed under seal pursuant to the Protective Order entered in this case.

/s/ Michael R. Rueckheim
Michael R. Rueckheim